6-19-00 Re-issue

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PTO/SB/50 (4/98)
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# REISSUE PATENT APPLICATION TRANSMITTAL

*Address to:*
**Assistant Commissioner for Patents**
**Box Patent Application**
**Washington, DC 20231**

| | |
|---|---|
| *Attorney Docket No.* | 95-C-153RE (1678-26) |
| *First Named Inventor* | David C. McClure |
| *Original Patent Number* | 5,767,709 |
| *Original Patent Issue Date (Month/Day/Year)* | 06/16/98 |
| *Express Mail Label No.* | EK111030111US |

**APPLICATION FOR REISSUE OF:** *(check applicable box)* [x] *Utility Patent* [ ] *Design Patent* [ ] *Plant Patent*

## APPLICATION ELEMENTS

1. [ ] * Fee Transmittal Form *(PTO/SB/56)* *(Submit an original, and a duplicate for fee processing)*
2. [x] Specification and Claims (*amended, if appropriate*)
3. [x] Drawing(s) *(proposed amendments, if appropriate)*
4. [x] Reissue Oath / Declaration (original or copy) *(37 C.F.R. § 1.175)(PTO/SB/51 or 52)*
5. Original U.S. Patent
   - [ ] Offer to Surrender Original Patent *(37 C.F.R. § 1.178)* *(PTO/SB/53 or PTO/SB/54)*
   - *or*
   - [ ] Ribboned Original Patent Grant
   - [ ] Affidavit / Declaration of Loss *(PTO/SB/55)*
6. Original U.S. Patent currently assigned?
   - [x] Yes [ ] No

   *(If Yes, check applicable box(es))*
   - [ ] Written Consent of all Assignees *(PTO/SB/53 or 54)*
   - [x] 37 C.F.R. § 3.73(b) Statement [x] Power of Attorney

## ACCOMPANYING APPLICATION PARTS

7. [ ] Foreign Priority Claim *(35 U.S.C. 119)* *(if applicable)*
8. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
9. [ ] English Translation of Reissue Oath/Declaration *(if applicable)*
10. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
11. [x] Preliminary Amendment
12. [x] Return Receipt Postcard *(MPEP 503)* *(Should be specifically itemized)*
13. [x] Other: Request for Drawing Change; Cert. of Express Mail

** NOTE FOR ITEMS 1 & 10: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

## 14. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [x] *Correspondence address below*

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| | | | |
|---|---|---|---|
| *NAME (Print/Type)* | Bryan A. Santarelli | *Registration No. (Attorney/Agent)* | 37,560 |
| *Signature* | | *Date* | 06/15/00 |

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentee: David Charles McClure

Patent No.: 5,767,709

Title: SYNCHRONOUS TEST MODE INITIALIZATION

Issued: June 16, 1998

Atty Dk No.: 95-C-153

Reissue Application

Applicant: David Charles McClure

Serial No.:

Title: SYNCHRONOUS TEST MODE INITIALIZATION

Filing Date: June 15, 2000

Atty Dk No.: 95-C-153RE (1678-26)

CERTIFICATE OF MAILING OR TRANSMISSION

"Express Mail" mailing label number: EK111030111US

Date of Deposit: June 15, 2000

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Kelly Pedersen
Signature

**ASSENT OF ASSIGNEE**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

STMicroelectronics, Inc. (formerly known as SGS-Thomson Microelectronics, Inc.), assignee of U.S. Patent No. 5,767,709, consents to the filing of reissue application No. _____ (or the present application, if filed with the initial application papers) for the reissue of U.S. Patent No. 5,767,709.

STMicroelectronics, Inc.

_____

Lisa K. Jorgenson
Director of Intellectual Property

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentee: David Charles McClure

Patent No.: 5,767,709

Title: SYNCHRONOUS TEST MODE INITIALIZATION

Issued: June 16, 1998

Atty Dk No.: 95-C-053

Reissue Application

Applicant: David Charles McClure

Serial No.:

Title: SYNCHRONOUS TEST MODE INITIALIZATION

Filing Date: June 15, 2000

Atty Dk No.: 95-C-053RE (1678-26)

CERTIFICATE OF MAILING OR TRANSMISSION

"Express Mail" mailing label number: EK111030111US

Date of Deposit: June 15, 2000

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Kelly Pedersen
Signature

**FIRST PRELIMINARY AMENDMENT**

June 15, 2000

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

In the Drawings:

The Applicant respectfully requests the Examiner to transfer FIGS. 1, 1a, and 3 - 6 from the file of the issued `709 patent to the reissue file, and requests approval of the amendment to FIG. 2 as requested in the enclosed Request for Drawing Change.

In the Specification:

In the Abstract, line 8, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Lines 9 – 10, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Starting in column 1, line 6, through column 2, line 6, please insert:

--[The subject matter of the present application is related to copending U.S. application Ser. No. 08/173,197, filed Dec. 22, 1993, titled "Improved Static Memory Long Write Test", attorney docket no. 93-C-82, copending U.S. application Ser. No. 08/172,854, filed Dec. 22, 1993, titled "Stress Test Mode", attorney docket no. 93-C-56 all of which are assigned to SGS-Thomson Microelectronics, Inc. and expressly incorporated herein by reference.

Additionally, the following pending U.S. patent applications by David Charles McClure entitled:

"Architecture Redundancy", Ser. No. 08/582,484 (Attorney's Docket No. 95-C-136), and

"(Redundancy Control", Ser. No. 08/580,827 (Attorney's Docket No. 95-C-143), which were both filed on Dec. 29, 1995, and have the same ownership as the present application, and to that extent are arguable related to the present application, which are herein incorporated by reference;

and entitled:

"Test Mode Activation and Data Override", Ser. No. 08/587,709 (Attorney's Docket No. 95-C-137),

"Pipelined Chip Enable Control Circuitry and Methodology", Ser. No. 08/588,730_(Docket No. 95-C-138),

"Output Driver Circuitry Having a Single Slew Rate Resistor", Ser. No. 08/588,988 (Docket No. 95-C-139),

"Synchronized Stress Test Control", Ser. No. 08/589,015 (Docket No. 95-C-142),

"Write Pass Through Circuit", Ser. No. 08/588,662 (Attorney's Docket No. 95-C-144), "Data-Input Device for Generating Test Signals on Bit and Bit-Complement Lines", Ser. No. 08/588,762 (Attorney's Docket No. 95-C-145),

"Synchronous Output Circuit", Ser. No. 08/588,901 (Attorney's Docket No. 95-C-146),

"Write Driver Having a Test Function", Ser. No. 08/589,141 (Attorney's Docket No. 95-C-147),

"Circuit and Method for Tracking the Start of a Write to a Memory Cell", Ser. No. 08/589,139 (Attorney's Docket No. 95-C-148),

"Circuit and Method for Terminating a Write to a Memory Cell", Ser. No. 08/588,737 (Attorney's Docket No. 95-C-149),

"Clocked Sense Amplifier with Wordline Tracking", Ser. No. 08/587,728 (Attorney's Docket No. 95-C-150),

"Memory-Row Selector Having a Test Function", Ser. No. 08/589,140 (Attorney's Docket No. 95-C-151),

"Device and Method for Isolating Bit Lines from a Data Line", Ser. No. 08/588,740 (Attorney's Docket No. 95-C-154),

"Circuit and Method for Setting the Time Duration of a Write to a Memory Cell", Ser. No. 08/587,711 (Attorney's Docket No. 95-C-156),

"Low-Power Read Circuit and Method for Controlling A Sense Amplifier", Ser. No. 08/589,024, U.S. Pat. No. 5,619,466 (Attorney's Docket No. 95-C-168),

"Device and Method for Driving a Conductive Path with a Signal", Ser. No. 08/587,708 (Attorney's Docket No. 169),

and the following pending U.S. patent applications by Mark A. Lysinger entitled:

"Burst Counter Circuit and Method of Operation Thereof", Ser. No. 08/589,023 (Attorney's Docket No. 95-C-141),

"Switching Master/Slave Circuit", Ser. No. 08/588,648 (Attorney's Docket No. 96-C-03),

which have the same effective filing data and ownership as the present application, and to that extent are arguably related to the present application, are incorporated herein by reference.]

The subject matter of the present application is related to U.S. Pat. No. 5,577,051, titled "Improved Static Memory Long Write Test", U.S. Pat. No. 5,835,427, titled "Stress Test Mode", all of which are assigned to SGS-Thomson Microelectronics, Inc. and expressly incorporated herein by reference.

Additionally, the following U.S. patents by David Charles McClure entitled:

"Architecture Redundancy", U.S. Pat. No. 5,612,918, and

"Redundancy Control", U.S. Pat. No. 5,790,462, which were both filed on Dec. 29, 1995, and have the same ownership as the present application, and to that extent are arguably related to the present application, which are herein incorporated by reference;

and entitled:

"Test Mode Activation and Data Override", Ser. No. 08/587,709,

Ser. No. 09/457,558 which is a continuation of Ser. No. 08/587,709,

Ser. No. 09/454,800 which is a divisional of Ser. No. 08/587,709,

"Pipelined Chip Enable Control Circuitry and Methodology", U.S. Pat. No. 5,701,275,

U.S. Pat. No. 5,798,980 which is a divisional of U.S. Pat. No. 5,701,275,

"Output Driver Circuitry Having a Single Slew Rate Resistor", U.S. Pat. No. 5,801,563,

"Synchronized Stress Test Control", U.S. Pat. No. 5,712,584,

"Write Pass Through Circuit", U.S. Pat. No. 5,657,292,

"Data-Input Device for Generating Test Signals on Bit and Bit-Complement Lines", U.S. Pat. No. 5,845,059,

"Synchronous Output Circuit", U.S. Pat. No. 5,619,456,

"Write Driver Having a Test Function", U.S. Pat. No. 5,745,432,

"Circuit and Method for Tracking the Start of a Write to a Memory Cell", Ser. No. 08/589,139 (since abandoned),

U.S. Pat. No. 5,808,960 which is a continuation of Ser. No. 08/589,139,

"Circuit and Method for Terminating a Write to a Memory Cell", Ser. No. 08/588,737 (since abandoned),

U.S. Pat. No. 5,825,691 which is a continuation of Ser. No. 08/588,737,

"Clocked Sense Amplifier with Wordline Tracking", U.S. Pat. No. 5,802,004,

U.S. Pat. No. 5,828,622 which is a divisional of U.S. Pat. No. 5,802,004,

"Memory-Row Selector Having a Test Function", Ser. No. 08/589,140 (since abandoned),

U.S. Pat. No. 5,848,018 which is a continuation of Ser. No. 08/589,140,

"Device and Method for Isolating Bit Lines from a Data Line", U.S. Pat. No. 5,691,950,

"Circuit and Method for Setting the Time Duration of a Write to a Memory Cell", U.S. Pat. No. 5,864,696,

U.S. Pat. No. 6,006,339 which is a divisional of U.S. Pat. No. 5,864,696,

"Low-Power Read Circuit and Method for Controlling A Sense Amplifier", U.S. Pat. No. 5,619,466,

"Device and Method for Driving a Conductive Path with a Signal", Ser. No. 08/587,708 (since abandoned),

U.S. Pat. No. 5,896,336 which is a continuation of Ser. No. 08/587,708,

U.S. Pat. No. 5,883,838 which is a divisional of Ser. No. 08/587,708,

and the following U.S. patents by Mark A. Lysinger entitled:

"Burst Counter Circuit and Method of Operation Thereof", Ser. No. 08/589,023 (since abandoned),

U.S. Pat. No. 5,805,523 which is a continuation of Ser. No. 08/589,023,

"Switching Master/Slave Circuit", U.S. Pat. No. 5,783,958,

which have the same effective filing data and ownership as the present application, and to that extent are arguably related to the present application, are incorporated herein by reference.--

In column 3, line 3, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Line 5, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Line 51, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Line 53, please replace "latch (flip-flop)" with --latch [(flip-flop)]flip-flop--.

Line 60, please replace "and then are allowed to sequentially conduct" with --[and then are allowed to sequentially conduct]--.

In column 4, line 35, please replace "Control bar signal **14** and Control signal **18**" with --Control bar derivative signal [**14**]**23** from Node **4** and Control derivative signal [**18**]**27** from node **3**--.

Line 39, please replace "**14**" with --[**14**]**23**--.

Line 42, please replace "**18**" with --[**18**]**27**--.

Line 49, please replace "**23**" with --[**23**]**21**--.

Line 67, please replace "signal" with --derivative signal--.

In column 5, line 1, please replace "**3**" with --[**3**]**4**--, "signal" with --derivative signal--, and "**4**" with --[**4**]**3**.

Line 4, after "Conversely," please insert -- when the Power-On-Reset signal **16** goes to a low logic state, and--.

Line 5, please replace both instances of "signal" with --derivative signal—and please replace "go to" with –[go to]remain at--.

Line 9, please replace both instances of "signal" with --derivative signal--.

Line 14, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 19, please replace "which is allowed to device conduct" with --[which is allowed to device conduct]--.

Line 20, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 24, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 33, please replace "passgate" with --passgates 90 and--.

Line 34, please insert --derivative-- before "signal".

Line 36, please replace "13" with --[13]21--.

Line 40, please insert --derivative-- before both instances of "signal".

Line 43, please replace "high" with --[high]low--.

Line 44, please replace "**12**" with --[**12**]**38**-- and "turning off" with --[turning off]thus latching--.

Line 52, please replace "inverter" with --[inverter]invert--.

Line 64, after "Address", please insert --bar--, and please replace "116" with --[116]128--.

Line 66, after "Address", please insert --bar--, and please replace "116" with --[116]128--.

In column 6, line 32, after "transistors" please insert --**158**,--.

Line 27, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 35, please replace "**152**" with --[**152**]**162**--.

Line 36, please replace "**152**" with --[**152**]**162**--.

Line 55, please replace "signal **12**" with --derivative signal [**12**]**38**--.

Line 59, please replace "signal **12**" with --derivative signal [**12**]**38**--.

In column 7, line 6, please replace the second occurrence of "**216**" with --[**216**]**214**--.

In the Claims:

Please add the following new claims.

18. A method, comprising:

powering up an integrated circuit;

loading a first data bit into a master latch during the powering up of the integrated circuit;

generating a second data bit from the first data bit;

latching the first data bit in the master latch after powering up the integrated circuit; and

loading the second data bit into a slave latch after powering up the integrated circuit.

19. The method of claim 18 wherein powering up the integrated circuit comprises powering up the integrated circuit in a test mode.

20. The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to the first data bit.

21. The method of claim 18 wherein generating the second data bit comprises generating the second data bit equal to the complement of the first data bit.

22. The method of claim 18 wherein generating the second data bit comprises generating the second data bit during and after the powering up of the integrated circuit.

23. The method of claim 18 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise generating the clock signal having a second clock stage.

24. The method of claim 18 wherein:

loading the first data bit into the master latch comprises generating a clock signal inside the integrated circuit, the clock signal having a first clock state; and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise generating the clock signal having a second clock state.

25. A method, comprising:

generating a power-on reset signal having a first reset state during a power up of an integrated circuit;

generating the power-on reset signal having a second reset state after the power up of the integrated circuit;

loading a first data bit into a master latch in response to the power-on reset signal having the first state;

generating a second data bit from the first data bit;

storing the first data bit in the master latch in response to the power-on reset signal having the second state; and

loading the second data bit into a slave latch in response to the power-on reset signal having the second state.

26. The method of claim 25 wherein:

generating the power-on reset signal having the first state comprises generating the power-on reset signal having the first state when an integrated-circuit supply voltage has a first level; and

generating the power-on reset signal having the second state comprises generating the power-on reset signal having the second state when the supply voltage has a second level.

27. The method of claim 25 wherein:

generating the power-on reset signal having the first state comprises generating the power-on reset signal having the first state during a power up of the integrated circuit in a test mode; and

generating the power-on reset signal having the second state comprises generating the power-on reset signal having the second state after the power up of the integrated circuit in the test mode.

28. The method of claim 25 wherein generating the second data bit comprises generating the second data bit in response to the power-on reset signal having either the first state or the second state.

29. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating a test signal having a first test state.

30. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating multiple test signals each having a first test state.

31. The method of claim 25 wherein storing the first data bit in the master latch and loading the second data bit into the slave latch comprise:

generating a test signal having a test state; and

generating a clock signal having a clock state in response to the test signal having the test state.

32. The method of claim 25 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state in response to the power-on reset signal having the first reset state; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,

generating a test signal having a test state, and

generating the clock signal having a second clock state in response to the test signal having the test state.

33. The method of claim 25 wherein:

loading the first data bit into the master latch comprises,

generating a clock signal having a first clock state in response to the power-on reset signal having the first reset state,

generating a test signal having a test state, and

generating the first data bit in response to the test signal; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise generating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the test state.

34. The method of claim 25 wherein:

loading the first data bit into the master latch comprises,

generating a clock signal having a first clock state in response to the power-on reset signal having the first reset state,

generating a test signal having a first test state, and

generating the first data bit in response to the test signal; and

storing the first data bit in the master latch and loading the second data bit into the slave latch comprise,

generating the test signal having a second test state, and

generating the clock signal having a second clock state in response to the power-on reset signal having the second reset state and the test signal having the second test state.

35. A method, comprising:

powering up an integrated circuit;

loading a first data bit into a master latch during the powering up of the integrated circuit;

latching the first data bit in the master latch after powering up the integrated circuit; and

loading the first data bit into a slave latch after powering up the integrated circuit.

36. The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state; and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock stage.

37. The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal inside the integrated circuit, the clock signal having a first clock state; and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock state.

## REMARKS

Claims 1 - 37 are pending in this broadening reissue application.

The Applicant has amended the drawings to correct a minor error as discussed in the enclosed Request for Drawing Change.

The Applicant has amended the specification to correct minor errors.

The Applicant has added new method claims 18 - 37, which the Applicant believes broaden the scope of protection to his invention.

The Applicant has added no new matter to the reissue application.

In light of the foregoing, original claims 1 – 17 as issued and new claims 18 – 37 are in condition for full allowance, and that action is respectfully requested.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicant's attorney, Bryan Santarelli, at (425) 455-5575.

DATED this 15th day of June, 2000.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP

Bryan A. Santarelli
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(425) 455-5575

Enclosures

# SYNCHRONOUS TEST MODE INITALIZATION

## CROSS REFERENCE TO RELATED APPLICATIONS

The subject matter of the present application is related to copending U.S. application Ser. No. 08/173,197, filed Dec. 22, 1993, titled "Improved Static Memory Long Write Test", attorney docket no. 93-C-82, copending U.S. application Ser. No. 08/172,854, filed Dec. 22, 1993, titled "Stress Test Mode", attorney docket no. 93-C-56 all of which are assigned to SGS-Thomson Microelectronics, Inc. and expressly incorporated herein by reference.

Additionally, the following pending U.S. patent applications by David Charles McClure entitled:

"Architecture Redundancy", Ser. No. 08/582,484 (Attorney's Docket No. 95-C-136), and

"(Redundancy Control", Ser. No. 08/580,827 (Attorney's Docket No. 95-C-143), which were both filed on Dec. 29, 1995, and have the same ownership as the present application, and to that extent are arguable related to the present application, which are herein incorporated by reference;

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"Pipelined Chip Enable Control Circuitry and Methodology", Ser. No. 08/588,730_(Docket No. 95-C-138).

"Output Driver Circuitry Having a Single Slew Rate Resistor", Ser. No. 08/588,988 (Docket No. 95-C-139).

"Synchronized Stress Test Control", Ser. No. 08/589,015 (Docket No. 95-C-142).

"Write Pass Through Circuit", Ser. No. 08/588,662 (Attorney's Docket No. 95-C-144). "Data-Input Device for Generating Test Signals on Bit and Bit-Complement Lines", Ser. No. 08/588,762 (Attorney's Docket No. 95-C-145).

"Synchronous Output Circuit", Ser. No. 08/588,901 (Attorney's Docket No. 95-C-146).

"Write Driver Having a Test Function", Ser. No. 08/589,141 (Attorney's Docket No. 95-C-147).

"Circuit and Method for Tracking the Start of a Write to a Memory Cell", Ser. No. 08/589,139 (Attorney's Docket No. 95-C-148).

"Circuit and Method for Terminating a Write to a Memory Cell", Ser. No. 08/588,737 (Attorney's Docket No. 95-C-149).

"Clocked Sense Amplifier with Wordline Tracking", Ser. No. 08/587,728 (Attorney's Docket No. 95-C-150).

"Memory-Row Selector Having a Test Function", Ser. No. 08/589,140 (Attorney's Docket No. 95-C-151).

"Device and Method for Isolating Bit Lines from a Data Line", Ser. No. 08/588,740 (Attorney's Docket No. 95-C-154).

"Circuit and Method for Setting the Time Duration of a Write to a Memory Cell", Ser. No. 08/587,711 (Attorney's Docket No. 95-C-156).

"Low-Power Read Circuit and Method for Controlling A Sense Amplifier", Ser. No. 08/589,024, U.S. Pat. No. 5,619,466 (Attorney's Docket No. 95-C-168).

"Device and Method for Driving a Conductive Path with a Signal", Ser. No. 08/587,708 (Attorney's Docket No. 169).

and the following pending U.S. patent applications by Mark A. Lysinger entitled:

"Burst Counter Circuit and Method of Operation Thereof", Ser. No. 08/589,023 (Attorney's Docket No. 95-C-141).

"Switching Master/Slave Circuit", Ser. No. 08/588,648 (Attorney's Docket No. 96-C-03),
which have the same effective filing data and ownership as the present application, and to that extent are arguably related to the present application, are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

The present invention relates generally to the testing of integrated circuit devices, and more specifically to the testing of synchronous integrated circuit devices having a stress test mode or other test mode.

Stress test modes are commonly used in modern synchronous integrated circuit devices to subject the integrated circuit device to various types of tests which "stress" the device. It is important to stress various element and signals of the device for maximum fault coverage. For instance, the external clock signal supplied to the integrated circuit device is an important signal to test because it controls many of the gates contained within the device. Thus, for maximum fault coverage of the device, it is important to stress the external clock signal both at a low logic state and a high logic state. Difficulties are encountered in trying to establish the logic states of the device during a stress test mode. These difficulties are encountered in a memory cell stress test mode of the device, in which all rows and columns are enabled and bitlines true or bitlines complement of the memory cell are pulled to power supply voltage Vss, or in a periphery stress test mode in which all rows and columns of the device are disabled. The difficulty lies in the fact that master/slave latches on the inputs of the integrated circuit device do not allow data to flow all the way through the device since only one master latch or one slave latch will conduct at a time.

Another prior art problem encountered with synchronized integrated circuit test modes is that entering a test mode after the integrated circuit device has been powered-up can result in device latch-up. Once the device powers-up, it has initialized to a certain voltage, such as 3 volts or 5 volts. Transition to a test mode from this voltage condition causes huge current spikes which can result in device latch-up as all the rows, columns, bitlines, etc. of the device simultaneously switch from a normal operating mode to a test mode. It would thus be desirable to enter a test mode upon power-up of the device in order to avoid possible device latch-up.

There is thus an unmet need in the art to be able to initialize the entire data path of an integrated circuit device in a test mode during device power-up and to be able to adequately test the external clock signal of the device or a derivative clock signal thereof in both a high logic state and a low logic state.

## SUMMARY OF THE INVENTION

It is an object of the present invention to initialize the entire data path of an integrated circuit device during a test mode upon power-up of the synchronous integrated circuit device.

It is further an object of the present invention to adequately test the external clock signal or internal clock signals associated with the external clock signal of the synchronous integrated circuit device.

Therefore, according to the present invention, the entire data path of the synchronous integrated circuit device is initialized in a test mode upon power-up of the integrated circuit device. Upon power-up of the integrated circuit device in the test mode, a clock signal (either an external

clock signal or an associated internal clock signal) is internally clocked. As the clock signal goes to a low logic state upon power-up of the device, a master latch (flip-flop) element of the integrated circuit device is loaded with data and is allowed to conduct; a slave latch (flip-flop) element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock, the slave latch element is loaded with data and is allowed to conduct.

## BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a schematic diagram of a clock input buffer, according to a preferred embodiment of the present invention;

FIG. 1*a* is a schematic diagram of a TTL (transistor transistor logic) cell, according to the preferred embodiment of the present invention;

FIG. 2 is a schematic diagram of an address input buffer, according to the preferred embodiment of the present invention;

FIG. 3 is a schematic diagram of row address driver circuitry, according to the preferred embodiment of the invention;

FIG. 4 is a schematic diagram of word line and block select latch circuitry, according to the preferred embodiment of the invention;

FIG. 5 is a schematic diagram of word line select circuitry, according to the preferred embodiment of the present invention; and

FIG. 6 is a schematic diagram of local wordline driver circuitry, according to the preferred embodiment of the present invention.

## DESCRIPTION OF THE INVENTION

The entire data path of a synchronous integrated circuit device is initialized in a test mode upon power-up of the integrated circuit device. Upon power-up of the integrated circuit device in the test mode, a clock signal (either an external clock signal or an associated internal clock signal) is internally clocked. As the clock signal goes to a low logic state upon power-up of the device, a master latch (flip-flop) element of the integrated circuit device is loaded with data and is allowed to conduct; a slave latch (flip-flop) element of the integrated circuit device does not conduct. As the clock signal goes to a high logic state, the data in the master latch is latched. Also upon the high logic state of the clock, the slave latch element is loaded with data and is allowed to conduct. Using the present invention, both the master and slave latch elements are sequentially loaded with the correct data state and then allowed to sequentially conduct.

Conduction of the master latch elements and conduction of the slave latch elements initializes an address path of the integrated circuit device such that either no columns or rows of the integrated circuit device are selected or such that all columns or rows of the integrated circuit device are selected. If all columns and rows of the integrated circuit device are selected, all bitlines true of the integrated circuit device are

held at a first voltage level and all bitlines complement of the integrated circuit device are held at a second voltage level.

FIGS. **1** and **1***a* illustrate the clock control circuitry which controls the external clock or derivative signal thereof of the synchronous integrated circuit device. FIGS. **2** to **6** illustrate the address control circuitry which are driven by the clock circuitry of FIG. **1**. Referring to FIG. **1**, a schematic diagram of a clock input buffer **10**, according to a preferred embodiment of the present invention, is shown. Clock input buffer **10** is provided with Clock signal **12**, Power-On-Reset signal **16**, Control bar signal **14** and Control signal **18**. Clock signal **12** is equal to the external clock signal provided to a clock pin of the integrated circuit device or is a derivative signal thereof and is provided as an input signal to TTL clock cell **22**, shown in FIG. **1***a*. The power-on-reset signal is an internally generated signal which changes logic state once a threshold value of positive power supply Vcc is passed as Vcc rises. Control signal **18** and Clock bar signal **14** are provided to NAND logic gate **36** as input signals. The output signal of NAND logic gate **36** is inverted by inverter **34** before being presented to a second NAND logic gate **32** as an input signal. The second input signal of NAND logic gate **32** is Power-On-Reset signal **16**. The output signal of NAND logic gate **32** feeds both NAND logic gates **26** and **30**. A second input signal to NAND logic gate **26** is Control bar signal **14** and a second input signal to NAND logic gate **30** is Control signal **18**. The output signal of NAND logic gate **26** is inverted by inverter **24** and the output signal of inverter **24** is an input signal to TTL Clock Cell **22**. The output signal of NAND logic gate **30** is inverted by inverter **28** and the output signal of inverter **28** is another input signal to TTL Clock Cell **22**. The output signal of TTL Clock Cell **22** is inverted by inverter **20** to produce Clock Derivative signal **38**.

Control bar signal **14** and Control signal **18** control TTL cell **22** shown in FIG. **1***a*. TTL cell **22** contains the following elements: p-channel MOS transistors **50**, **52** and **58** and n-channel MOS transistors **54**, **56** and **60**. The gates of transistors **50** and **60** are supplied with Control bar signal **14**. The gates of transistors **52** and **54** are supplied with Clock signal **12**, and the gates of transistors **56** and **58** are supplied with the Control signal **18**. A first source/drain of transistor **50** and a first source/drain of transistor **58** are connected to power supply voltage Vcc as shown. A second source/drain of transistor **50** is connected to a first source/drain of transistor **52**. A second source/drain of transistor **52** is connected to a first source/drain of transistor **54**, a first source/drain of transistor **60** and a second source/drain of transistor **58** to form output signal **23** on Node **5**. A second source/drain of transistor **54** is connected to a first source/drain of transistor **56**. A second source/drain of transistor **56** is connected to a second source/drain of transistor **60** and power supply voltage Vss.

When in the periphery stress test mode Control bar signal **14** and Control signal **18** are a high logic state. Referring again to FIG. **1**, during power-up of the integrated circuit device Power-On-Reset signal **16** pulses high. When Power-On-Reset signal **16**, Control bar signal **14** and Control signal **18** are all a high logic state, Node **1** of FIG. **1** is a high logic state and Node **2** is a low logic state, which means that Node **3** and Node **4** are both a low logic state. Once Power-On-Reset signal **16** goes to a low logic state, Node **2** goes to a high logic state. Node **3** and Node **4** are equal to the logic state of Control bar signal **14** and Control signal **18** both of which are now a high logic state.

Referring once more to FIG. **1***a*, during power-up in a periphery stress test mode, Control' bar signal **23** (shown at

Node 3 of FIG. 1) and Control' signal 27 (shown at Node 4 of FIG. 1) are both a low logic state and signal 21 at Node 5 is forced to a high logic state. This gives the appearance that Clock input signal 12 was a low logic state. Conversely, when Control' bar signal 23 and Control' signal 27 go to high logic states, signal 21 is forced to a low logic state which gives the appearance that Clock signal 12 was a high logic state. Thus, a high logic state on controls signals Control' bar signal 23 and Control' signal 27 during a periphery stress test mode forces the equivalent of a high going clock input. During a memory cell stress test mode, the equivalent of a low going clock input is forced. Upon power-up of the device, Power-On-Reset signal 16 goes high and Clock signal 12 is forced to a low logic state during which the master latch of the device is loaded with data and allowed to conduct. Following completion of the power-on reset cycle, Power-On-Reset signal 16 goes low and data is latched into the master latch; also data is loaded into the slave latch which is allowed to device conduct. Using the circuitry of FIG. 1*a*, the state of Clock signal 12 is forced to the desired logic state during a test mode, either a periphery stress test mode or a memory cell stress test mode.

The operation of FIG. 1*a* to force the condition of the Clock signal 12 as desired may be further illustrated with reference to a second input buffer circuit. Referring to FIG. 2, a schematic diagram of an address input buffer 70, according to the preferred embodiment of the present invention, is shown. Input buffer 70 includes the following elements: TTL (transistor transistor logic) cell 22, inverters 84, 88, 92 and 94, and passgates 90 and 96. The details of TTL cell 22 are similar to those shown in FIG. 1*a*. Input buffer 70 contains a master latch 95 comprised of elements inverter 92, inverter 94 and passgate 96. Input buffer 70 is supplied with the following input signals: Clock signal 38, Control bar signal 14, IN data signal 15, Control signal 18 and Clock bar signal 13 and generates output signal 98.

When Control bar signal 14 and Control signal 18 are both a high logic state, signal 72 at Node 1 is a low logic state. Because of the way the TTL cell of FIG. 1*a* forces Clock signal 38 to the desired logic state, Clock signal 38 is initially a low logic state but will ultimately go to a high logic state so that the master latch 95 initially conducts, thereby forcing signal 98 to a high logic state. Clock signal 12 will then go to a high logic state, turning off master latch 95.

Signal 98 propagates to Row Address Driver circuitry 100 of FIG. 3, according to the preferred embodiment of the invention. Row address driver circuitry 100 is composed of inverters 110, 112, 114, 124 and 126, p-channel MOS transistor 118, n-channel MOS transistor 122, and passgate 120. Signal 98 from FIG. 1 is provided to a series of inverters 110, 112 and 114 which delay and inverter signal 98 to produce Row Address signal 116. Signal 98 is also presented to passgate 120 which is controlled by Address Override-P signal 104 and Address Override-N signal 106. The output signal of passgate 120 is pulled up towards Vcc by p-channel transistor 118 whose gate is controlled by Rows On bar signal 102 and is pulled down towards Vss by n-channel transistor 122 whose gate is controlled by Rows Off signal 108. The output signal of passgate 120 passes through two inverters 124 and 126 to become Row Address bar signal 128. Row Address bar signal 128 is the inverse of Row Address signal 116. Rows On bar signal 102 forces Row Address signal 116 on (in an asserting condition) when it is a low logic state in the test mode and Rows Off signal 108 forces Row Address signal 116 off (not in an asserting condition) when it is a high logic state in the test mode.

P-channel MOS transistor **118** and n-channel MOS transistor **122** act as row address override devices in the test mode.

Rows On bar signal **102** and Rows Off signal **108** are controlled based upon which type of test mode being entered: a memory cell stress mode in which all rows are enabled or a periphery stress mode in which all the rows are disabled. Based on the logic states of signal **98**, Rows On bar signal **102** and Rows Off signal **108** and further based upon the fact that Address Override-P signal **104** is a high logic state and Address Override-N signal **106** is a low logic state in any test mode, Row Address signal **116** and Row Address bar signal **128** are both forced to a high logic state in a memory cell stress mode in an asserting condition for the Word Line and Block Select Latch circuitry **130** of FIG. **4** or are both forced to a low logic state in a periphery stress mode.

The Row Address signal **116** generated by FIG. **3** feeds the Word Line and Block Select Latch circuitry **130** shown in FIG. **4**, according to the preferred embodiment of the invention. In addition to Row Address signal **116**, circuitry **130** is supplied with Smart Clock signal **132**, Smart Block Select signal **134**, Block Address**0** signal **136**, Block Address**1** signal **138** and Block Address**2** signal **140**, and Reset signal **192**. Circuitry **130** generates Row signal **190** and Block Select bar signal **194**. Smart Clock signal **132** is a high-going narrow pulse generated from the rising edge of Clock signal **12** and Smart Block Select signal **134** is a derivative signal of Smart Clock signal **132**. The elements of circuitry **130** include: inverters **142**, **146**, **148**, **150**, **154**, **164**, **166** and **186**; passgates **144**, **152** and **162**; NAND logic gate **160**; p-channel MOS transistors **156**, **168**, **170**, **172**; and n-channel MOS transistors **174**, **176**, **178**, **180**, **182** and **184**.

Row Address signal **116** is supplied by FIG. **3** to the input terminal of inverter **142**. Smart Clock signal **132** is provided to a control terminal of both passgates **144** and **152** as shown and accordingly controls passgates **144** and **152**; it additionally is provided to the input terminal of inverter **150**. Smart Block Select signal **134** is an input signal to passgate **152** which is indirectly controlled by Block Address signals **136**, **138** and **140**. Block Address**0** signal **136** is provided to the gates of transistors **168**, **174** and **184**. Block Address**1** signal **138** is provided to the gates of transistors **178**, **170** and **180**. Block Address**2** signal **140** is provided to the gates of transistors **182**, **172** and **176**.

The output terminal of **142** provides an inverted row address signal to passgate **144**. The output of slave passgate **144** is provided to the input terminal of inverter **146** which produces Row output signal **190**. The output terminal of inverter **150** controls a control terminal of both passgates **144** and **162** while Smart Clock signal **132** controls the other control terminal of passgates **144** and **162** as shown.

Following the powering-up of the integrated circuit device which is controlled by Power-On-Reset signal **16**, Power-On-Reset signal **16** goes low and Clock signal **12** goes from a low logic state to a high logic state. This also causes Smart Clock signal **132** to go to the high logic state since Smart Clock signal **132** is a derivative signal of Clock signal **12**, as previously discussed. A high logic state of Smart Clock signal **132** causes slave latch member **144** to load in data supplied by Row Address signal **116** and to conduct. Thus, the conduction of slave latch **144** follows the conduction of the master latch of FIGS. **1** and **1***a*.

The Row signal **190** and Block Select bar signal **194** generated by circuitry **130** are supplied to Word Line Select circuitry **200** of FIG. **5**, according to the preferred embodiment of the present invention. In addition to signals **190** and

194 circuitry **200** is provided with Row bar signal **202**, which is the inverse of Row signal **190**. The elements of circuitry **200** include NOR logic gates **204** and **208**; and inverters **206**, **210** and **212**. Circuitry **200** produces signal Row Driver Line even bar signal **218**, Row Driver Line odd bar signal **216** and Block Select signal **216** (the inverse signal of Block Select bar signal **194**).

Row Driver Line odd bar signal **216** and Row Driver Line even bar signal **218** from circuitry **200** feeds the Local Wordline Driver circuitry **220** of FIG. **6**, according to the preferred embodiment of the present invention. Circuitry **220** in addition to signals **216** and **218** is provided with a Master Word Line signal **222** and Word Line Driver Enable signal **224**. The elements of circuitry **220** include p-channel MOS transistors **226**, **228**, **236** and **238**; n-channel MOS transistors **230** and **240**; and inverters **232** and **242**. Circuitry **220** produces Local Wordline odd signal **234** and Local Wordline even bar signal **246**. When Row Driver Line odd bar signal **216** and Row Driver Line even bar signal **218** are both a high logic state, Local Wordline Odd signal **234** and Local Wordline even bar signal **246** will be off (a low logic state). Since Local Wordline Odd signal **234** and Local Wordline even bar signal **246** are the local wordlines of the device, all wordlines of the device are off.

The internal clocking of the synchronous integrated circuit device described above provides several advantages over the prior art. The entire data path of a synchronous integrated circuit device may be set up based upon exercising only the internally generated power-on-reset signal of the integrated circuit device. It is not necessary, as it was in the prior art, to exercise the clock device pin in order to enter or affect the test mode. Since the clock signal is internally forced, testing of the clock signal in two logic states, both a high logic state and a low logic state, is possible. Thus, the clock is testing in both a memory cell stress test mode and in a periphery stress test mode. The exercise of the clock signal in both logic states is an important advantage since the clock signal is typically connected to many gates of the synchronous integrated circuit device.

Since the test mode is entered internally and the clock signal is internally forced, the test is more reliable than it is to exercise the clock device pin to enter the test mode; one need not worry about pin continuity problems during testing since the device is internally clocked. Also, because the clock pin need not be probed to enter the test mode, the number of pins which must be exercised by test equipment is reduced and thus more devices may be simultaneously tested due to the reduced pin count.

A further advantage of the present invention is provided by powering-up the integrated circuit device in the test mode, rather than switching to the test mode subsequent to powering-up the device as is done in the prior art. Powering-up the device in the test mode prevents the huge current spikes which may result in a latch-up condition of the device.

The present invention is desirable in any system or device employing synchronous integrated circuits. Thus it is envisioned that the present invention is suitable for use in a number of device types, including: memory devices such as SRAM (static random access memory), DRAM (dynamic random access memory) and BRAM (burst RAM) devices;

programmable devices; logic devices; gate arrays; ASICs (application specific integrated circuits); and microprocessors. The present invention is further suitable for use in any system or systems which employ such devices types.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. For instance, the address path circuitry shown in the figures is but one example of how the circuitry and methodology of the present invention may be implemented.

What is claimed is:

1. A method of internally controlling a clock signal of an integrated circuit device such that a data path of the integrated circuit device is initialized in a test mode, comprising the steps of:

upon a power-up condition in the test mode of the integrated circuit device forcing the clock signal of the integrated circuit device to a first logic state, thereby causing a master element of the integrated circuit device to load in first data and to conduct; and

upon completion of the power-up condition forcing the clock signal of the integrated circuit device to a second logic state, thereby latching In the first data to the master element and causing a slave element of the integrated circuit device to load in second data generated by the master element and to conduct.

2. The method of claim 1, wherein the first logic state is a low logic state and the second logic state is a high logic state.

3. The method of claim 1, wherein the power-up condition of the integrated circuit device is controlled by a power-on-reset signal of the integrated circuit device.

4. The method of claim 3, wherein the power-on-reset signal is an internally generated signal which changes logic state once a threshold value of a positive power supply is passed as the positive power supply rises.

5. The method of claim 1, wherein the clock signal of the integrated circuit device is an external clock signal of the integrated circuit device or a derivative signal of the external clock signal.

6. The method of claim 1, wherein the master element of the integrated circuit device is a master latch element and the slave element is a slave latch element.

7. The method of claim 1, wherein the master element of the integrated circuit device is a master flip-flop element and the slave element is a slave flip-flop element.

8. The method of claim 1, wherein upon the power-up condition of the integrated circuit device, the clock signal is internally clocked.

9. The method of claim 1, wherein when the master element is conducting the slave element does not conduct and when the slave element is conducting the master element does not conduct.

10. The method of claim 1, wherein the test mode is entered upon the power-up condition of the integrated circuit device.

11. The method of claim 1, wherein the data path is an address path.

12. The method of claim 1, wherein in the test mode the integrated circuit device is tested at a voltage above a normal operating voltage of the integrated circuit device.

13. The method of claim 12, wherein the clock signal is tested in both the first logic state and the second logic state at the voltage.

14. The method of claim 1, wherein the integrated circuit device is a synchronous clocked device.

15. The method of claim 1, wherein conduction of the master element and conduction of the slave element initializes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are not selected.

16. The method of claim 1, wherein conduction of the master element and conduction of the slave element initial-

izes an address path of the integrated circuit device such that a plurality of columns and a plurality of rows of the integrated circuit device are selected.

17. The method of claim 16, wherein a plurality of bitlines true of the integrated circuit device are held at a first voltage level and a plurality of bitlines complement of the integrated circuit device are held at a second voltage level.

* * * * *

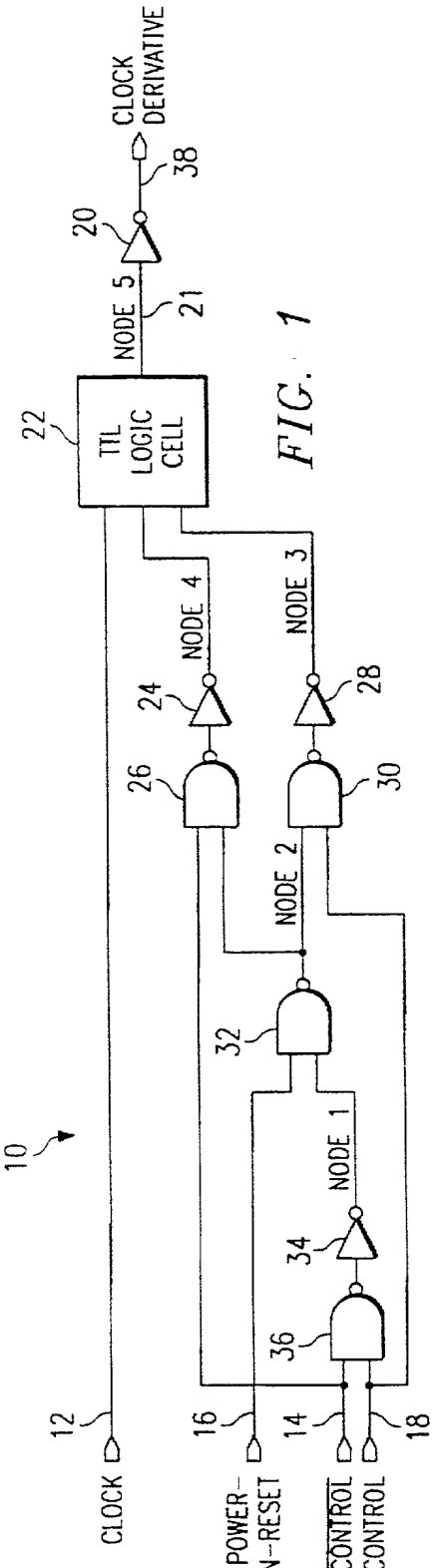
CLOCK DERIVATIVE
38
20
NODE 5
21
22
TTL LOGIC CELL
NODE 4
NODE 3
24
28
26
30
NODE 2
32
NODE 1
34
36
10
12
16
14
18
CLOCK
POWER-ON-RESET
CONTROL
CONTROL

FIG. 1

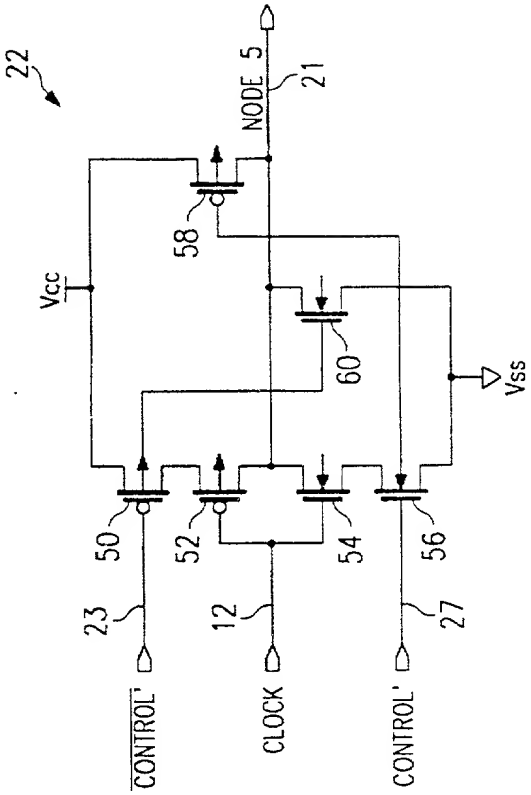
22
NODE 5
21
58
Vcc
60
Vss
50
52
54
56
23
12
27
CONTROL
CLOCK
CONTROL

FIG. 1a

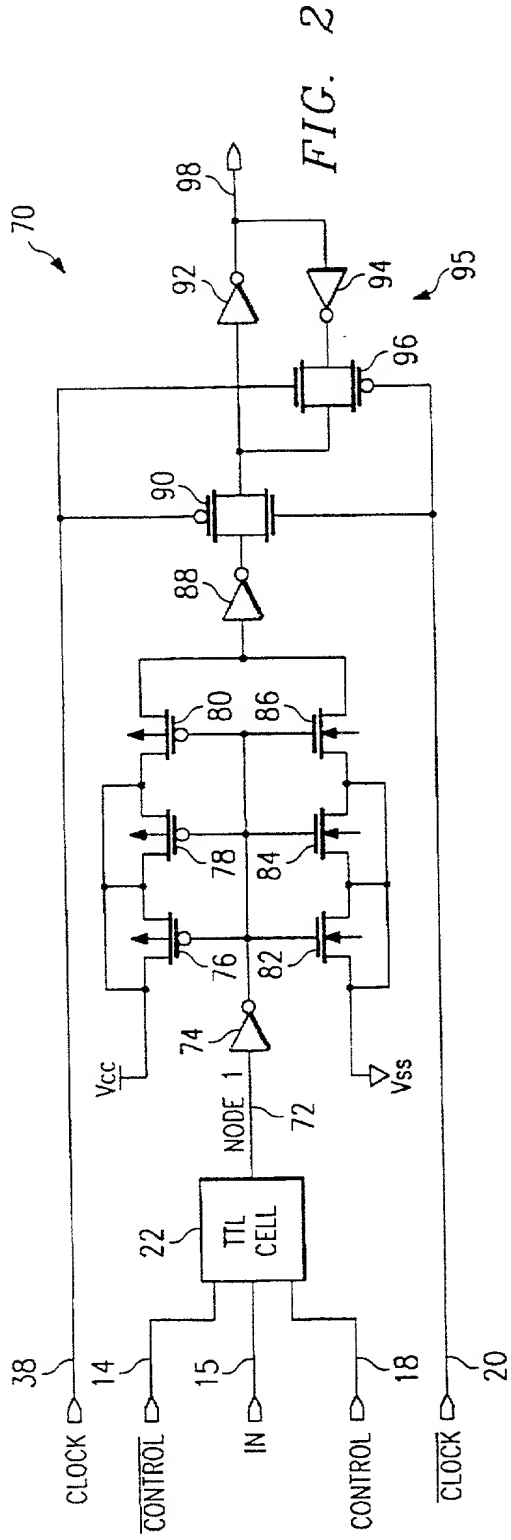
70
98
92
94
95
96
90
88
80
86
78
84
76
82
74
Vcc
Vss
NODE 1
72
22
TTL CELL
38
14
15
18
20
CLOCK
CONTROL
IN
CONTROL
CLOCK

FIG. 2

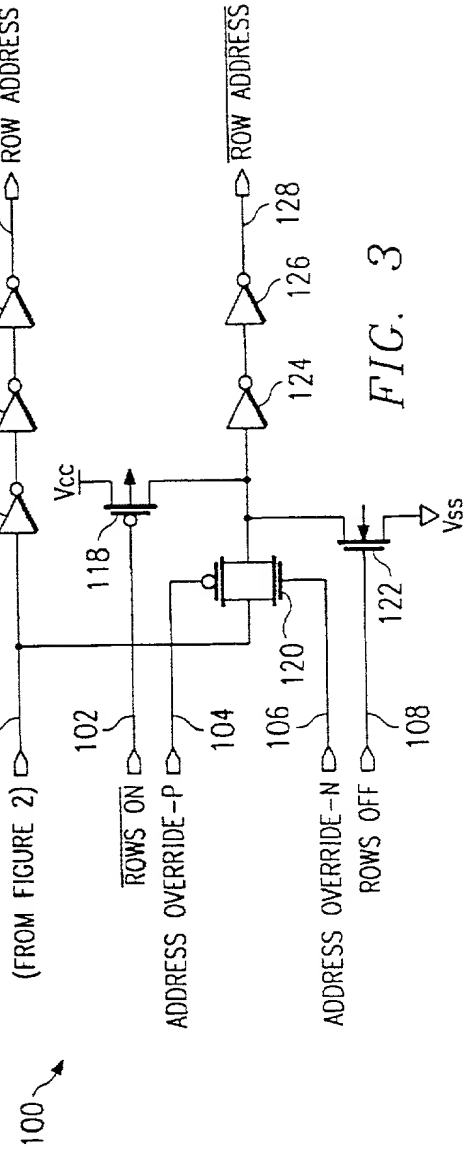
100
98
(FROM FIGURE 2)
110
112
114
116
ROW ADDRESS
Vcc
118
102
ROWS ON
104
ADDRESS OVERRIDE-P
106
ADDRESS OVERRIDE-N
120
122
ROWS OFF
108
124
126
128
ROW ADDRESS
Vss

FIG. 3

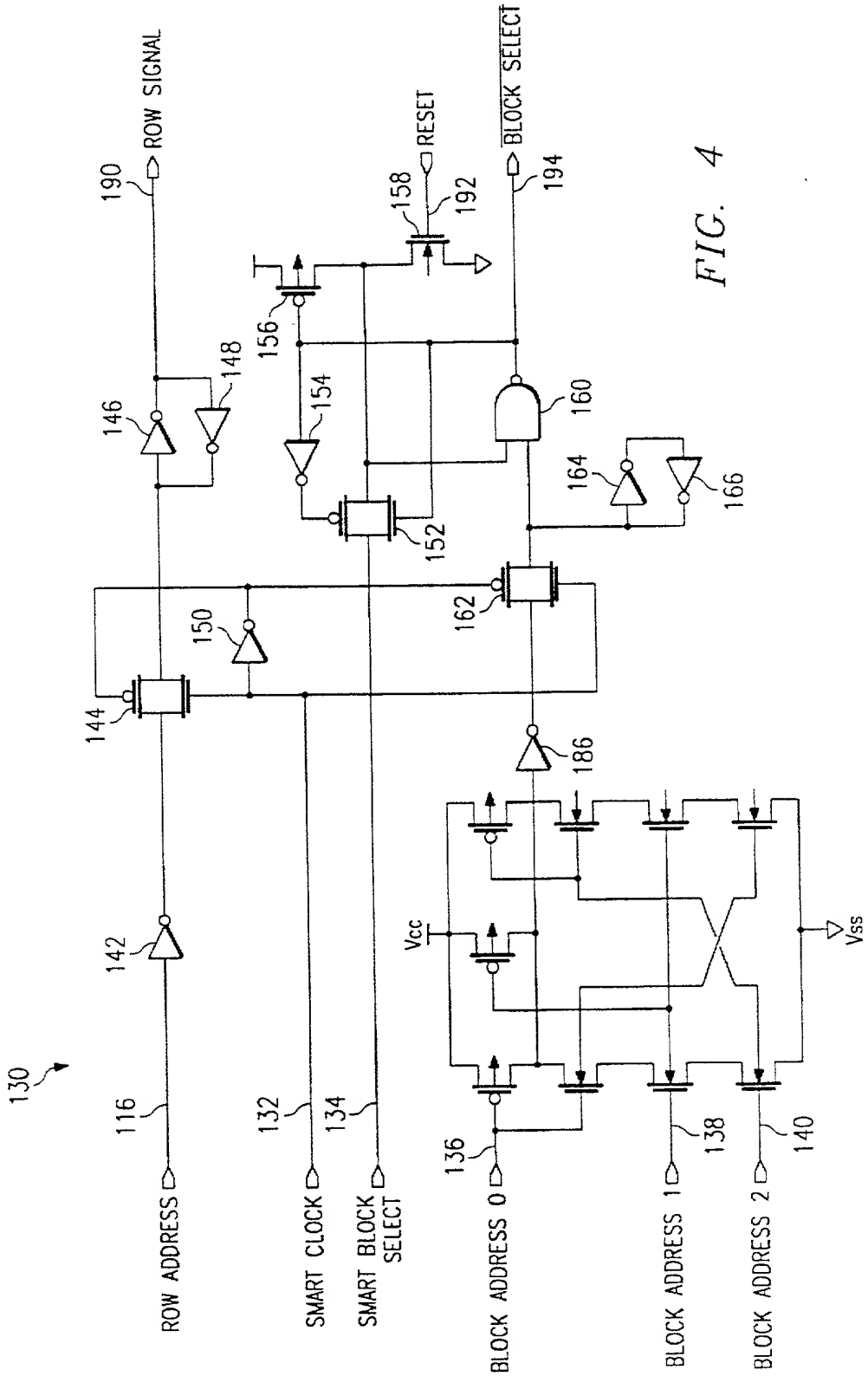
130
116
ROW ADDRESS
132
SMART CLOCK
134
SMART BLOCK SELECT
136
BLOCK ADDRESS 0
138
BLOCK ADDRESS 1
140
BLOCK ADDRESS 2
142
144
146
148
150
152
154
156
158
160
162
164
166
186
190
ROW SIGNAL
192
RESET
194
BLOCK SELECT
Vcc
Vss

FIG. 4

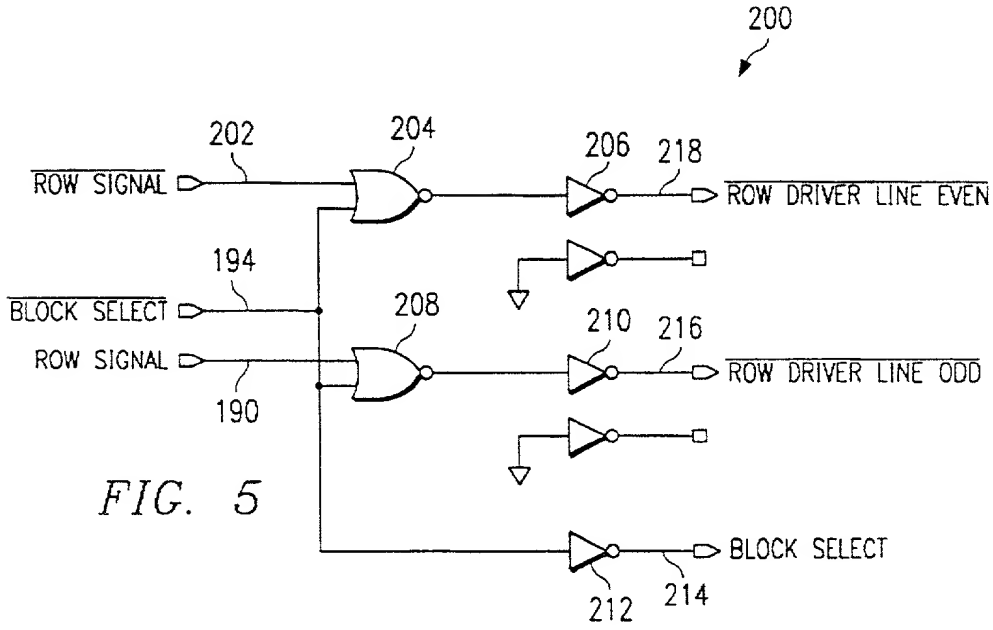
200
202
204
206
218
ROW SIGNAL
ROW DRIVER LINE EVEN
194
BLOCK SELECT
208
210
216
ROW SIGNAL
ROW DRIVER LINE ODD
190
BLOCK SELECT
212
214

FIG. 5

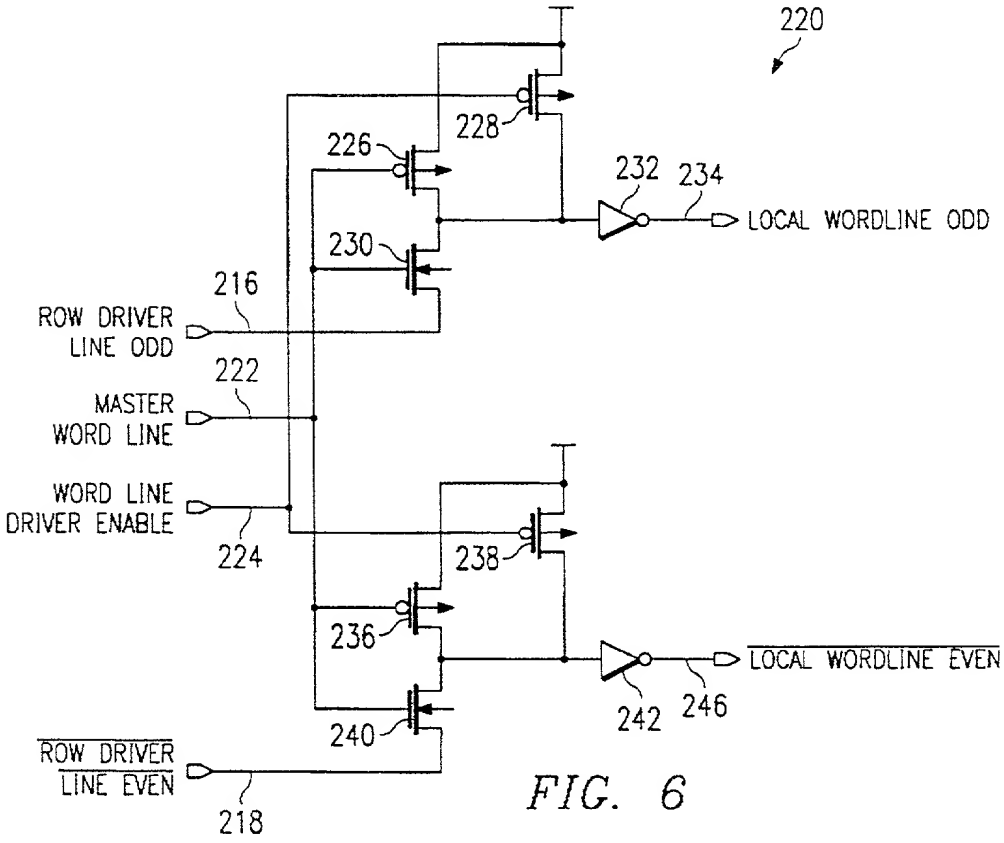
220
228
226
232
234
LOCAL WORDLINE ODD
230
216
ROW DRIVER
LINE ODD
222
MASTER
WORD LINE
WORD LINE
DRIVER ENABLE
224
238
236
LOCAL WORDLINE EVEN
242
246
240
ROW DRIVER
LINE EVEN
218

FIG. 6

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentee: David Charles McClure

Patent No.: 5,767,709

Title: SYNCHRONOUS TEST MODE INITIALIZATION

Issued: June 16, 1998

Atty Dk No.: 95-C-053

Reissue Application

Applicant: David Charles McClure

Serial No.:

Title: SYNCHRONOUS TEST MODE INITIALIZATION

Filing Date: June 15, 2000

Atty Dk No.: 95-C-053RE (1678-26)

CERTIFICATE OF MAILING OR TRANSMISSION

"Express Mail" mailing label number: EK111030111US

Date of Deposit: June 15, 2000

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR, Section 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Box PATENT APPLICATION, Washington, D.C. 20231 by

Kelly Pedersen
Signature

**REQUEST FOR DRAWING CHANGE**

ASSISTANT COMMISSIONER FOR PATENTS:

Applicant requests approval of the changes shown in red ink in the enclosed Figures 3 and 4. No new matter has been added to the enclosed figures.

Respectfully submitted,

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Enclosures: Figures 3 and 4

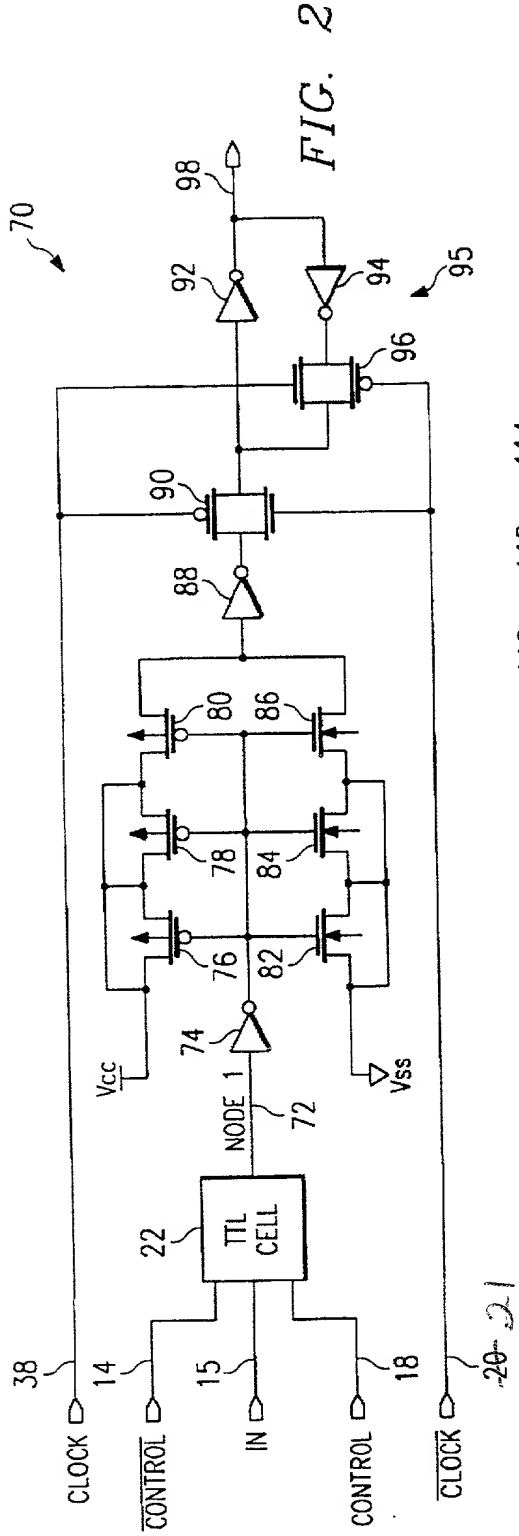


FIG. 2

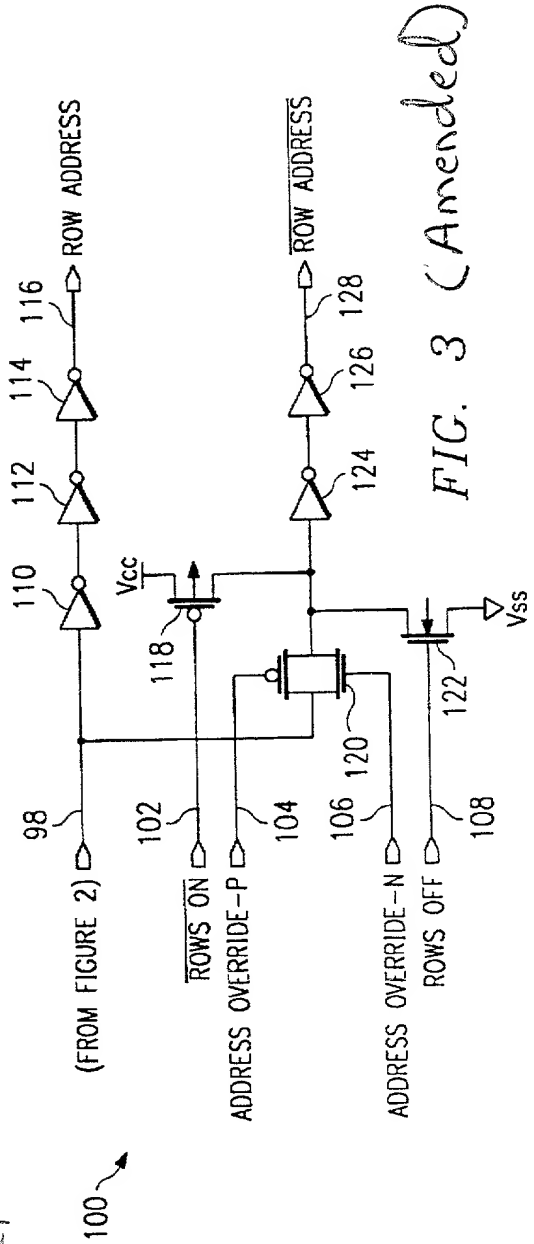


FIG. 3 (Amended)

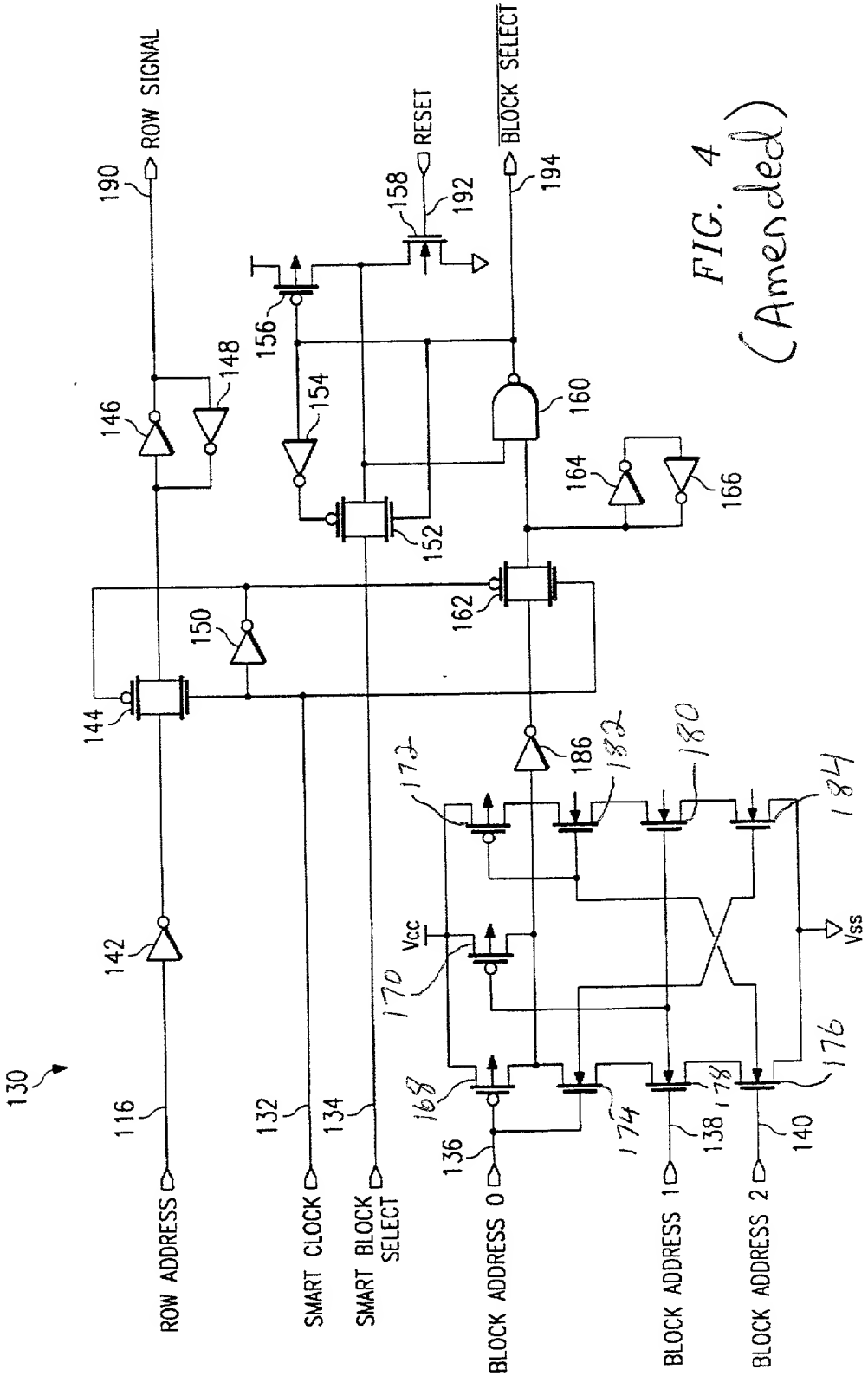


FIG. 4 (Amended)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Original Patent

Patentee: David Charles McClure

Patent No.: 5,767,709

Title: SYNCHRONOUS TEST MODE INITIALIZATION

Issued: June 16, 1998

Atty Dk No.: 95-C-153

Reissue Application

Applicant: David Charles McClure

Serial No.:

Title: SYNCHRONOUS TEST MODE INITIALIZATION

Filing Date: June 15, 2000

Atty Dk No.: 95-C-153RE (1678-26)

## REISSUE APPLICATION DECLARATION BY THE INVENTOR

As a below named inventor, I hereby declare:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are listed below) of the subject matter that is claimed in patent number 5,767,709, granted June 16, 1998, and for which a reissue patent is sought on the invention entitled:

SYNCHRONOUS TEST MODE INITIALIZATION

the specification of which

☑ is attached hereto.

☐ was filed on _____ as reissue application number _____ and was amended on _____ (if applicable). If the filing date, amendment date, or reissue application number are not included when I execute this Declaration, I authorize the below appointed attorney(s) and/or agents(s) to insert the filing date, amendment date, or reissue application number when they become available.

I have reviewed and understand the contents of the above–identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all that apply.)

☑ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming less than he had the right to claim in the patent.

☐ by reason of other errors.

Errors upon which reissue is based are described as follows:

I have amended the specification, including the drawings, to correct errors therein.

I have added new claims 18 – 37 because I have recently come to believe that the "test mode" and "clock signal" limitations may render claims 1 – 17 unduly narrow.

All errors corrected in this reissue application arose without any deceptive intention on my part.

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: LISA K. JORGENSON, Reg. No. 34,845; THEODORE E. GALANTHAY, Reg. No. 24,122; ROBERT D. MCCUTCHEON, Reg. No. 38,717; JEFF MOY, Reg. No. 39,307; and all attorneys associated with Customer Number 000996.

Correspondence Address: Direct all communications about the application to:

Lisa K. Jorgenson
STMicroelectronics, Inc.
1310 Electronics Drive
Carrollton, Texas 75006-5039
Phone: (972) 466-6000
Fax: (972) 466-7044

I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof.

I do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country before my invention thereof.

I do not know and do not believe that the claimed invention was ever patented or made the subject of an inventor's certificate issued prior to the date of this application in any

country foreign to the United States of America on an application filed by me or my legal representatives or assigns.

I do not know and do not believe that the claimed invention was ever patented or described in any printed publication in any country more than one year prior to the filing date of the original U.S. application.

I do not know and do not believe that the claimed invention was ever in public use or on sale in the United States of America more than one year prior to the filing date of the original U.S. application.

I hereby claim the benefit of priority, under 35 U.S.C. § 119 and 35 U.S.C. § 120, of any foreign application(s) for patent or inventor's certificate on which priority was claimed in the above-identified issued patent.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon, or any patent to which this declaration is directed.

David Charles McClure _____

Full Name of Inventor

_____

Citizenship

_____

Residence

_____

Post Office Address (if different from Residence)

_____

Inventor's Signature

_____

Date

# CERTIFICATE UNDER 37 C.F.R. § 3.73(b)

Applicant: David Charles McClure

Reissue Application No.: Filed: June 15, 2000

For: PROGRAMMABLE BANDWIDTH VOLTAGE REGULATOR

STMicroelectronics, Inc., a corporaton
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, government agency, etc.)

certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

A. [X] An assignment from inventor of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel ____ Frame ____ (copy enclosed).

B. [ ] A chain of title from the inventor(s), of the patent application identified above, to the current assignees as shown below:

1. From:_____To: _____
The document was recorded in the Patent and Trademark Office at Reel____
Frame _____ or for which a copy thereof is attached.

2. From:_____ To: _____
The document was recorded in the Patent and Trademark Office at Reel ____
Frame ____ or for which a copy thereof is attached.

3. From:_____ To: _____
The document was recorded in the Patent and Trademark Office at Reel ____
Frame ____ or for which a copy thereof is attached.

[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignee identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignee.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: _____

Name: Lisa K. Jorgenson

Title: Director of Intellectual Property

Signature:_____

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION

PATENT NO. : 5,767,709

DATED : June 16, 1998

INVENTOR(S) : David Charles McClure

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page item [54], and column 1, line 3,

delete "INITALIZATION" and insert --INITIALIZATION--.

Signed and Sealed this

Fourteenth Day of September, 1999

*Attest:*

Q. TODD DICKINSON

*Attesting Officer*

*Acting Commissioner of Patents and Trademarks*